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Moisture requirements to reduce interfacial sub-oxides and lower hydrogen pre-bake temperatures for RPCVD Si epitaxy

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ABSTRACT

In silicon epitaxy technology, residual O/H_2O contamination requires thermal reduction using hydrogen pre-bakes to achieve atomically clean Si surfaces. This H_2 pre-bake leads to unwanted increase of thermal budget. The higher the level of interfacial O, the longer the pre-bake period and the higher the temperature have to be for removal of these contaminants. Moisture contamination from the pre-epi chamber etch (immediately before the wafer is loaded), with it's use of high flows of HCl, is identified as a major contributor to the area density of the interfacial O. Stringent control of moisture impurity in the HCl is required to reduce thermal budget. Ultra low temperature technology to desiccate HCl is used to achieve single digit ppb moisture resulting in lower temperature hydrogen pre-bakes than achieved with standard solid media-type HCl purification.

1. Introduction

Thermal budget is a major concern for all future generation 20 nm and beyond devices. Low temperature Epi processes are required to prevent Si agglomeration and excessive diffusion in FDSOI and FinFET technology. For epitaxy, much of the thermal budget is a result of a thermal H_2 pre-bake step designed to remove a remnant sub-oxide [1]. Reducing thermal budgets for the H_2 pre-bake step reliably to less than 750 °C has proven to be difficult to achieve in RPCVD. Lowering thermal budget for the H_2 pre-bake step has been one of the motivating factors for the Epi equipment OEM's to develop pre-clean modules attached to the cluster Epi tool.

Moisture and oxygen contamination are the primary determining factor in lowering thermal budget for epitaxy. Moisture is generally more problematic for epitaxy being a very polar molecule, and is not easily dislodged and pumped out from vacuum system surfaces as oxygen is. Fig. 1 depicts the reversible reaction of water with Si [2]. To maintain an oxide free surface in a low temperature Epi regime between 500 °C and 600 °C, the temperature range where future CMOS epitaxial film growth will occur, the water partial pressures should be $< 10^{-10}$ Torr. Typical H_2 pre-bakes temperatures to remove sub-oxides are carried out between 800 and 850 °C and the water partial pressures are relaxed to ~10^{-7} Torr. Even so, there is a great drive to lower the partial pressure for water, as the oxygen (from SiO) will desorb from the Si surface during the H_2 pre-bake at a higher rate. As standard dry pumps on an RPCVD system only achieve low milliTorr (1×10^{-3} Torr) base pressure and most of the residual partial pressures are from water, low ppb gas purification must be achieved at high gas flows to reduce chamber background and gas source moisture.

Past studies on moisture and it's effect on Si Epitaxy have dealt with overall moisture in the deposition process not moisture from any specific Epi process gas [3], or from either oxygen or moisture injected directly to simulate contamination from a process gas [4,8]. As semiconductor gases each interact differently with water, there is a need to study moisture contamination in the actual process gas. This work was undertaken to identify specific gas sources contributing to interfacial oxygen (not interstitial oxygen) contamination and to reduce that contamination through novel purification, which is the key to lowering the critical H_2 pre-bakes pre-bake temperature.

The most potential for generating high levels of moisture contamination resulting in high interfacial oxygen for low temperature (LT) epitaxy is a gas injected before the wafer is loaded

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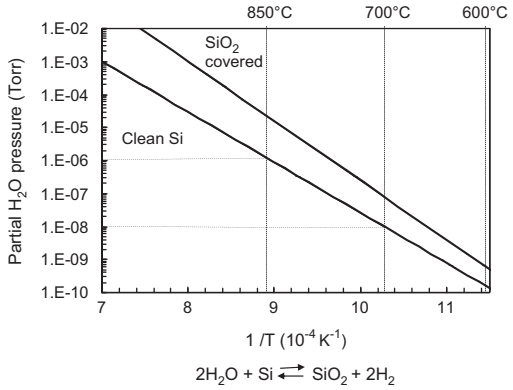

Fig. 1. Formation of SiO_2 as a function of H_2O partial pressure and temperature (reconstructed from [2]).

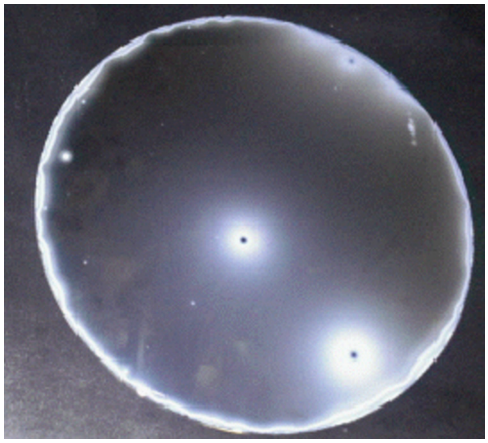

Fig. 3. Brite light tilted view of haze on perimeter of front side of Si substrate affected by ppm levels of HCl moisture.

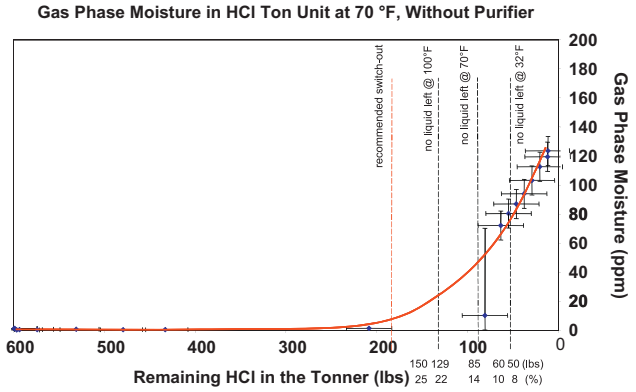

Fig. 2. Moisture levels in HCl tonner vs. weight.

into reaction chamber, that being HCl gas. A 99.999 semiconductor grade HCl has <1 ppm specification for moisture, but when the cylinder or bulk supply gets low or goes "liquid dry" moisture levels of tens of ppm can be experienced as shown in Fig. 2. Levels above 1 ppm have been shown to have a harmful effect on gas lines and components increasing the roughness of the electro-polishing potentially creating metals and particulate issues and eventually ruining gas panels [5]. In Fab environments, standard solid media-type purifiers for HCl are not capable of handling sustained high, or varying inlet challenges while maintaining the outlet purification specification of <200 ppb typical [6].

Moisture at ppm levels in the pre-epitaxy HCl chamber etch can lead to heavy etch pits in Si shown in Fig. 3 [6,7]. This severe condition is usually seen with H_2 pre-bakes >850 °C but typically leaves no interfacial O detected at the Epi/substrate growth interface. The hundreds of ppb level of moisture from HCl chamber etch, which is HCl introduced before the wafer is loaded, has been ignored as a potential oxidizer since the ppm level of moisture left no interfacial O. In this study, we do find a correlation for moisture in the hundreds of ppb level, in HCl from chamber etch, and elevated O at the Epi/substrate. Implication for LT epitaxy: interfacial O (atoms/cm^2) can reduce the strain of subsequently deposited Stressor films such as SiGe and SiC [8], whereas interstitial O (in the epilayers) can increase strain of SiGe films [9]. Etch pit density of defects increase exponentially with interfacial O at $>1\times10^{13}$ atoms/cm^2. Several studies have shown a relationship between the amount of oxygen present at the growth interface and the resulting etch pit density [10]. Photoluminescence also shows a loss of intensity when interfacial O is $>5\times10^{13}$ atoms/cm^2 [11]. Controlling the interfacial sub-oxide is critical to get repeatable growth rates in SEG. If the sub-oxide is $>5\times10^{13}$ atoms/cm^2 the onset of Epi growth can be reduced, and $>5\times10^{14}$ atoms/cm^2 the growth can stop entirely.

2. Experimental

B-doped 20–40 Ω/cm Si (100) substrates (backside polished) were used in all experiments. The native oxide was removed in dilute HF solution followed by an in-situ DI rinse. Queue time between the HF clean and loading into load lock was <1 h for all wafers. 3 pump downs were done in the load lock before the wafers were transferred to the wafer transfer chamber then to the reaction chamber.

All epitaxial layers were deposited in a commercially available reduced pressure chemical vapor deposition (RPCVD) single wafer reactor (SWR). This reactor was equipped with moisture contamination purification on all house gases (H_2, N_2, He) and also on most specialty gases. HCl gas was equipped with a solid media-type purifier along with a commercially available PICO-TRAP™ low temperature purifier that reduces moisture in HCl to less than 10 ppb as has been verified by both cavity ring down spectroscopy (CRDS) and tunable diode laser absorption spectroscopy (TDLAS) [12]. The low temperature purifier was facilitated such that it could be bypassed leaving only the solid media-type purifier in line see Fig. 4. The low temperature purifier uses the principles of chemisorption and physisorption to lower moisture in HCl to much lower levels than conventional solid media-type purifiers. Temperatures of ~−50 °C are needed to create a phase change in the water present in HCl at typical flows and pressures needed for epitaxy. The PICO-TRAP™ ultra low temperature purifier has been described in detail elsewhere [13,14].

HCl with a purity of 99.999% and <1 ppm moisture specification was used as the gas source. A TDLAS (Delta F Model 750) moisture analyzer was installed to sample in the foreline of the Epi chamber to measure the HCl's moisture level.

Sampling for moisture was made during the HCl chamber etch and continued just prior to wafer load into reaction chamber and Si deposition. As a chamber baseline, purified H_2 was measured separately and had a moisture measurement of ~5 ppb. Gas flows during moisture measurement in HCl was 20 slm purified H_2 and 20 slm HCl. The moisture analyzer was calibrated to analyze this 50/50 mixture. The HCl/H_2 mixture was measured with a solid media-type purifier in-line (Table 1), and then with a solid media resin-type purifier and low temperature purifier in-line (Table 2). The temperature of the reaction chamber was 1150 °C and the

pressure was near atmospheric, which are typical HCl etch conditions for commercial RPCVD reactors. The lowest moisture value obtained is recorded.

After exposing P-100 wafers to various levels of HCl moisture, several epitaxial H_2 pre-bake conditions all of 2 min duration were used followed by a 100 nm Si capping layers deposited at 650 °C at 80 Torr with silane chemistry. The Si capping layer is thick enough to get an accurate interfacial peak dose for O, without interference from the surface oxygen peak which is usually extends into epilayers 20–50 nm depending on SIMS conditions. SIMS was done on an Atomica 4100 at 2 keV with Cs^+ beam to analyze interfacial O/C.

3. Discussion

Moisture introduced with gas sources can remain for many minutes after the gas is turned off [3]. This long duration is because of the reaction chamber's water cooled front and rear flanges being only at 50–80 °C and the quartz chamber walls being at <300 °C during typical LT Epi processing as depicted in Fig. 5. Moisture from high volumes of HCl used during Epi chamber etch (preceeding deposition) is much more problematic than the typical low flows (sccm's) of HCl used for selective Epi growth (SEG). The effect is not just due to gas flow and level of impurities. HCl use in SEG, as long as Si surface is in etching mode the surface is not easily oxidized [15]. Experiments have been done flowing several liters of unpurified HCl (1 ppm moisture) during SEG growth with no interfacial oxygen contamination introduced. The situation is much different for HCl used in the chamber etch. When Si substrate is first loaded, the HCl has been mostly exhausted (non-etching regime) but moisture from the HCl remains in chamber as a potential oxidizer.

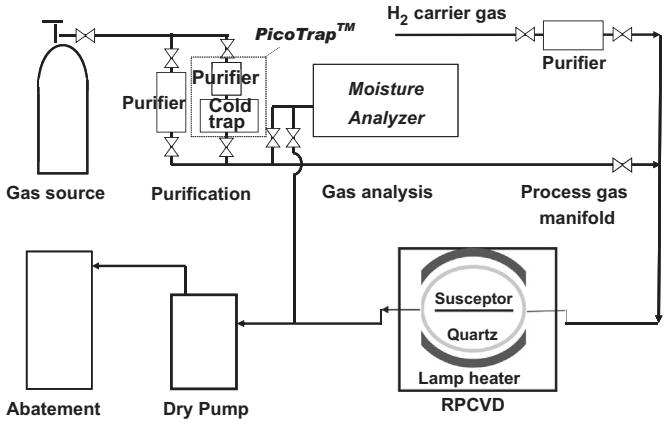

Fig. 4. Schematic of Single Wafer Epi Reactor and connections to the moisture analyzer.

Wafers are typically loaded at an indicated temperature of 700–750 °C. However, when the Si substrate is loaded into the chamber, the lamps are turned off, the Si substrate drops onto the susceptor, and the temperature drops very rapidly. In data shown in Fig. 5, we used upper and lower pyrometers to see exactly how much the wafer temperature changes when a bare Si wafer dropped onto susceptor. The bottom pyrometer is focused on the bottom of susceptor and the top pyrometer is focused on a P-Si substrate. Note the wafer temperature is as low as 500 °C (top pyrometer) immediately after loading onto susceptor. For over 60 s the temperature of the wafer is below 700 °C. In this temperature range Si is very reactive and any oxidizer introduced with high flow HCl gas during the preceding chamber etch step will rapidly reform a sub-oxide on the Si surface that becomes difficult to remove in subsequent H_2 pre-bake.

The results in Table 1 show oxygen area density in atoms/cm^2 for the series of H_2 pre-bakes and HCl moisture exposure. In this series of experiments only standard solid media-type purification is used. Notice different moisture measurements obtained on the same HCl gas source. HCl moisture can vary in the low hundreds of ppb range due to the hygroscopic nature of the gas. If there are final filters in common gas lines shared with HCl, as is typical in commercial Epi reactors the HCl will pick up moisture from those other gas or leak sources.

Table 1 demonstrates, as expected from Fig. 1, that as the pre-bake temperature is decreased the O interfacial area density increased. In the hundreds of ppb range only the 850 °C H_2 pre-bakes result in no detectable oxygen. Samples that are oxygen free for the bake conditions, 800 °C, and 825 °C, are where double digit ppb moisture can be achieved with the solid media-type purifier.

The results in Table 2 show oxygen area density in atoms/cm^2 for the series of H_2 pre-bakes and HCl moisture exposure. In this series of experiments the standard solid media-type purification is used in conjunction with the low temperature purifier designed to reduce HCl moisture near the moisture analyzer detectable limits. When switching from a solid media-type purifier to using solid media-type in conjunction with low temperature purifier, HCl was

Table 1
Solid media type HCl purifier moisture levels and interfacial O dose after series of H_2 Epi pre-bakes.

Sample	H_2 pre-bake temperature (°C)	HCl moisture (ppb)	HCl gas source (%)	Solid media type purifier	Interfacial O (atom/cm^2)	Background O (atom/cm^3)
1	850	246	99.999	Yes	Non-detect	5.00E17
2	825	208	99.999	Yes	7.00E12	1.80E18
3	800	141	99.999	Yes	4.74E13	1.50E18
3	775	115	99.999	Yes	5.83E13	2.00E18
4	750	133	99.999	Yes	7.23E13	2.00E18
5	825	85	99.999	Yes	Non-detect	2.00E17
6	800	86	99.999	Yes	Non-detect	2.00E17

Table 2
Solid media type HCl purifier and HCl cold trap moisture levels and interfacial O dose after a series of H_2 Epi pre-bakes.

Sample	H_2 pre-bake temperature (°C)	HCl moisture (ppb)	HCl gas source	Solid media type purifier	Pico-trap **−50** °C	Interfacial O (atom/cm^2)	Background O (atom/cm^3)
1	800	<8.9	99.999	Yes	Yes	Non-detect	2.00E17
2	775	<9.2	99.999	Yes	Yes	Non-detect	5.00E17
3	750	<8.5	99.999	Yes	Yes	2.60E12	5.00E17

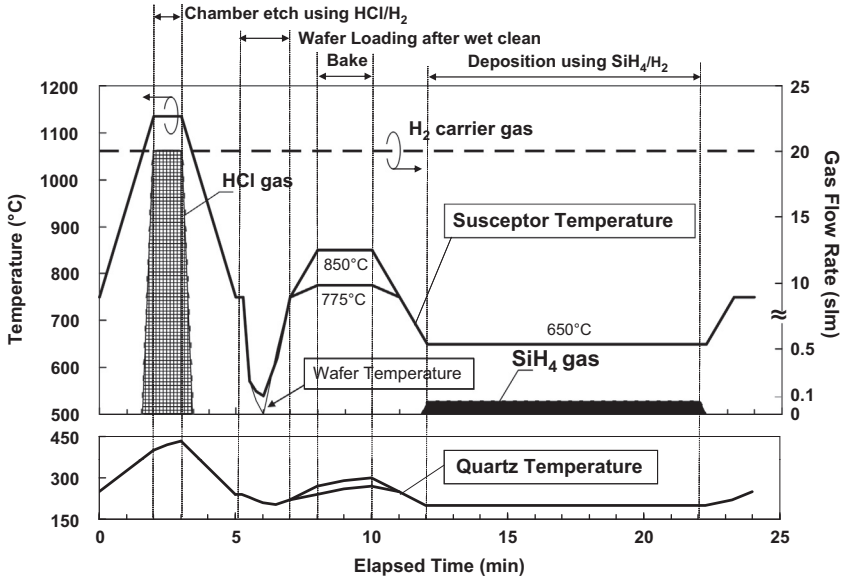

Fig. 5. Process sequence for chamber etch and deposition.

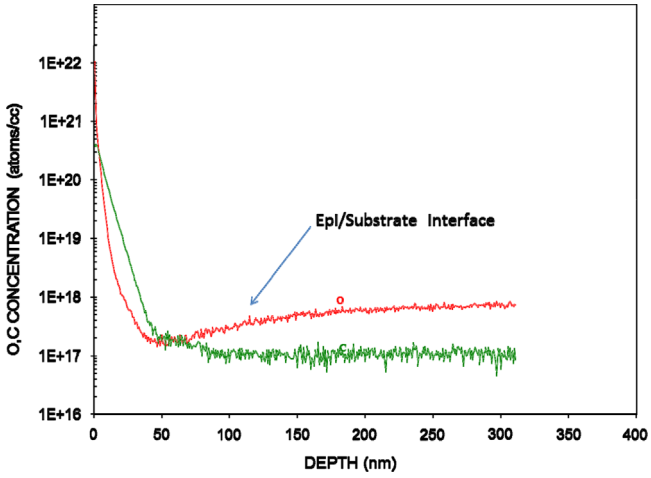

Fig. 6. 775C 2: SIMS data for 775 °C H_2 pre-bake with solid media HCl purifier used in conjunction with low temperature HCl purifier.

flowed for a period of time to condition the gas line. After this conditioning very stable single digit ppb levels of moisture were achieved.

Table 2 demonstrates that lowering moisture in HCl (used for HCl chamber etch) to single digit ppb levels enables the generation of O free substrate/Epi growth interfaces using H_2 pre-bakes temperatures as low as 775 °C as shown by the SIMS data in Fig. 6. At a lower pre-bake temperature of 750 °C only 2.5×10^{12} atoms/cm^2 O area density is remnant at the interface. This level of oxygen can be tolerated for most devices and does not typically lead to extended defects [12]. The results from Tables 1 and 2 show that solid media-type purification is adequate to achieve H_2 pre-bakes at 800 °C but to lower the bake temperature beyond this requires single digit ppb moisture levels. Low temperature purifier technology is needed to achieve H_2 prebake temperatures of 750 °C and lower.

4. Conclusion

Although moisture in epitaxy is ubiquitous in all sources, (wafers, vacuum system, and gas sources) HCl gas is particularly a concern because of it's hygroscopic nature and the large volumes (slm) of injection during Epi chamber etch immediately preceding wafer load into chamber. Moisture from HCl that is remaining from chamber etch can reside in the Epi reactor chamber ambient for several minutes increasing the O at the substrate/Epi growth interface resulting in high thermal budget H_2 pre-bakes. Lowering the HCl moisture to single digit ppb concentrations is needed to obtain H_2 pre-bakes as low as 750 °C and to control interfacial O to $< 1 \times 10^{12}$ atoms/cm^2. Low temperature purifier technology successfully desiccates HCl to enable lower temperature H_2 pre-bake temperatures of 750°C and lower.

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